OIPE JC34
MAR 2 3 2004
PATENT & TRADEMARK OFFICE

Image

AF / 1765 #

Please type a plus sign (+) inside this box → [+]

HDP/SB/21 based on PTO/SB/21 (08-00)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/017,942
Filing Date	December 13, 2001
First Named Inventor	Bradley Paul BARBER, et al.
Group Art Unit	1765
Examiner Name	A.K. Alanko
Attorney Docket Number	37310-000178/US

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment - Preliminary
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Letter to the Official Draftsperson and ( ) Sheets of Formal Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) ____
- [ ] After Allowance Communication to Group
- [ ] LETTER SUBMITTING APPEAL BRIEF AND APPEAL BRIEF (w/clean version of pending claims)
- [x] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) *(please identify below)*:

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Harness, Dickey & Pierce, P.L.C.	Attorney Name Gary D. Yacura	Reg. No. 35,416
Signature			
Date	March 23, 2004		

45,274

OIPE JC34 MAR 23 2004 PATENT & TRADEMARK OFFICE

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2004

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330

Complete if Known	
Application Number	10/017,942
Filing Date	December 13, 2001
First Named Inventor	Bradley Paul BARBER et al.
Examiner Name	A. K. Alanto
Art Unit	1765
Attorney Docket No.	37310-000178/US

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

Deposit Account Number: 08-0750

Deposit Account Name: Harness, Dickey & Pierce, P.L.C.

The Director is authorized to: *(check all that apply)*
☐ Charge fee(s) indicated below ☒ Credit any overpayments
☒ Charge any additional fee(s) during the pendency of this application
☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filling fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20 ** =	0	X		=	0
Independent Claims		-3 ** =	0	X		=	0
Multiple Dependent				X		=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

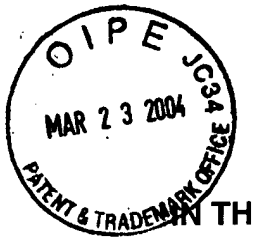
SUBTOTAL (3) ($) 330

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Gary D. Yacura	*Registration No. Attorney/Agent)*	35,416	*Telephone*	703-668-8000
Signature				*Date*	March 23, 2004

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing this form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.



PATENT
37310-000178/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Bradley Paul BARBER et al.	Conf. No.:	1470
Filing Date:	December 13, 2001	Group:	1765
Application No.:	10/017,942	Examiner:	A.K. Alanko
Title:	PROCESS FOR PACKAGING ELECTRONIC DEVICES USING THIN BONDING REGIONS		
Attorney Docket:	37310-000178/US		

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Mail Stop Appeal Brief

March 23, 2004

Dear Sir:

Appellants submit herewith their Brief on Appeal in triplicate as required by 37 C.F.R. 1.192.

03/24/2004 YPOLITE1 00000103 10017942
01 FC:1402 330.00 OP

TABLE OF CONTENTS

BRIEF ON BEHALF OF APPELLANT

In support of the Notice of Appeal filed January 23, 2004, appealing the Examiner's final rejection mailed December 8, 2003 of each of pending claims 1-12 of the present application which appear in the attached Appendix, Appellant hereby provides the following remarks.

(1) REAL PARTY IN INTEREST:

The real party in interest is Agere Systems, Inc, as evidenced by the assignment recorded at reel 012396, frame 0549.

(2) RELATED APPEALS AND INTERFERENCES:

No related appeals or interferences are known.

(3) STATUS OF THE CLAIMS:

Claims 1, 5 and 7-12 are pending, claims 2-4 and 6 having been canceled by the Amendment filed September 30, 2003, entered by the Examiner.

stand finally rejected under 35 U.S.C. §102(b) as being anticipated by.

Claims 1, 5 and 7-12 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurle et al. (U.S. Patent No. 6,106,735) in view of Sasaki et al. (U.S. Patent Application No. 2002/0017862).

(4) STATUS OF ANY AMENDMENT FILED SUBSEQUENT TO FINAL REJECTION:

The Amendment filed September 30, 2003 has presumably been entered. Appellants have made a minor clarifying amendment to claim 5 herein to change dependency from claim 4 (canceled) to claim 1. The Examiner and/or panel is kindly requested to enter this minor amendment to claim 5, as it reduces the number of issues on appeal.

(5) SUMMARY OF THE INVENTION:

Electronic devices fabricated in a large scale integrated (LSI) manner by thin film deposition, etching, etc., need to be packaged so as to be easily handled, and so as to be reliable in the variety of environmental conditions that are typically present in electronic systems. In the case of most simple electronic devices, polymer materials may be applied directly on the surface of a finished device for packaging. In the case of devices that are based on acoustic waves or mechanical motion, the part of the device that contains these acoustic waves must be isolated from intimate contact with packaging material, or the acoustic wave may be corrupted. Isolation may be achieved by forming a desired sized cavity of desired depth over the devices. It is desirable to form these cavities at the wafer scale, such that a multitude of devices are made in a batch process, lowering the cost per part.

One way to do this is to prepare a cap wafer to be bonded to another wafer that includes electronic devices such as integrated circuits (ICs). These wafers can then be bonded together, and thereafter the devices can be singulated (e.g., separated into individual devices). One such type of device is a thin film resonator (TFR). In a TFR, electrical signals are transformed into acoustic waves in a piezoelectric material, the acoustic waves resonate in a prepared structure where certain frequencies are reinforced, and electrical signals are again produced by the now changed acoustic waves to produce a filtering function.

The present invention provides a method of packaging sensory devices such as RF components and TFRs, where raised areas are formed on a cap wafer surface near the perimeter of a desired cavity region, such that the cap wafer surface may be bonded to a substrate surface containing the components. These raised areas can form an entire perimeter around the cavity region if the cavity is desired to be sealed, and specific sealing material such as glass frit can be used, if an impervious or hermetic seal is desired.

Figs. 1(a) and 1(b) illustrate bottom and side views of a section of a cap wafer in accordance with the invention. It is understood that this region can be repeated to fill the area of the cap wafer 100. As shown in Figure 1(a), a desired cavity region 102, is

defined by thin bonding strips or ridges 105 near the cavity region 102's perimeter. As shown, the bonding strips or ridges 105 enclose the cavity region 102 entirely, but it may be desirable to only place bonding material partially around the perimeter of the cavity region 102.

A sealing material 110 is placed on top of the bonding strips (or ridges) 105. The sealing material 110 bonds cap wafer100 to an electronic device wafer 125 upon which sits electrical connection (runner) 130, as shown in Fig. 1(b). Sealing material 110 may be a glass frit which is screen printed on the cap wafer 100.

Once the bonding strips 105 and sealing material 110 are formed, the cavity regions 102 thereby formed between cap wafer 100 and device wafer 125, are then singulated, or diced as is known in the art along a cut line 115. These wafers may be cut with a diamond-tipped wet saw along saw streets 120. The saw streets 120 are defined by the dashed lines in Fig. 1(a) around a cut line 115, and similarly in the vertical direction. Saw streets 120 preferably are about 100 micrometers wide, with the cut line 115 being about 30 micrometers wide.

Figure 2 illustrates an enlarged view of a raised ridge formed by the method in accordance with one embodiment of the invention. In this cross-sectional view, and specifically as shown in the enlarged view, a raised ridge 220 is formed inboard from the edge of the desired cavity region 200. Both the height and width of the ridge 220 may be adjusted to any desired dimension during initial fabrication of the cap wafer surface 202.

This flexibility in adjusting height and width of ridge 220 encourages a different separation between the surface of a device wafer (not shown) and the cap wafer surface 202 than would be possible if the designer was strictly relying on the thickness of deposited sealing (frit) material. Also, if that height is also a critical parameter, a more reproducible standoff could be produced if the frit material is applied so as to be a small fraction of the total height, where a greater ridge definition is utilized as the majority of the total height of the ridge 220. Further, the position of the ridge 220 on the cap wafer surface 202 can also be adjusted during fabrication of the cap wafer 200.

The raised ridges 220 may be lithographically formed by masking the surface and then performing an etching process during time of fabrication, as is known in the art. For example, if the cap wafer is silicon, photo-definable resist can be patterned in the shape of the ridges, and then fluorine-based etches can be used to remove material not masked by the resist. The resist can be removed after the etch, leaving the desired ridge pattern. These ridges 220 can then act as the bonding regions (or ridges) 105 onto which sealing material 110 is applied.

(6) ISSUES PRESENTED:

I. Issue 1: Is claim 1 rendered obvious by Kurle et al. in view of Sasaki et al.?

II. Issue 2: Are claims 8, 9 and 12 rendered obvious by Kurle et al. in view of Sasaki et al.?

III. Issue 3: Are claims 5 and 10 rendered obvious by Kurle et al. in view of Sasaki et al.?

IV. Issue 4: Is claim 11 rendered obvious by Kurle et al. in view of Sasaki et al.?

(7) GROUPING OF CLAIMS

Appellants respectfully request that the following claims be grouped together as indicated. Group I: claim 1; Group II: claims 8, 9 and 12; Group III: claims 5 and 10; Group IV: claim 11. Appellants respectfully assert that each of Groups I-IV are separately patentable for the reasons set forth below.

(8) ARGUMENTS WITH RESPECT TO THE ISSUES PRESENTED FOR REVIEW:

I. Issue 1: Is claim 1 rendered obvious by Kurle et al. in view of Sasaki et al.?

Appellants submit that neither Kurle et al. nor Sasaki et al. teach or suggest a method of packaging devices that operate based on acoustic waves, comprising at least the step of lithographically forming raised ridges on the cap wafer surface at areas near

a perimeter of a desired cavity region so that the raised ridges are a contiguous part of said cap wafer, in combination with the other steps recited in claim 1.

The Examiner already admits that Kurle et al. is deficient in teaching a particular method for packaging devices, alleging that Kurle et al. teaches "forming raised ridges 4 on the cap surface", yet states that it is not taught how the ridges are formed in Kurle et al. Appellants agree, Kurle et al. shows a web 4, but not how it is formed. Yet, the Examiner relies on FIGS. 4a-4e of Sasaki et al. to allege a teaching of lithographically forming raised ridges that would be attributable to Kurle et al. However, Appellants submit that Sasaki et al. forms a mixture of a frit glass layer 75 and alumina 701 over the flat dielectric film 72, and then forms a pattern in the frit glass/aluminum/dielectric film using a resist 76 to form division walls 74.

Accordingly, adopting the process shown in Sasaki et al. would not provide (a) first lithographically forming raised ridges on the cap wafer surface at areas near a perimeter of a desired cavity region so that the raised ridges are a contiguous part of said cap wafer, and then (b) printing a glass frit material on the raised ridges, (already formed) as recited in claim 1. One would have to substantially alter the process in Kurle et al., eliminating the application of bonding frit strips 5 to web 4, since the frit strips would already have been applied. For at least this reason, Appellants submit that the references fails to teach each and every recited feature of the claim, as required by 35 U.S.C. §103.

Notwithstanding the above, the rejection is deficient as against the weight of case precedent as directed to obviousness rejections under 35 U.S.C. §103. The claimed invention is directed to a method of packaging electronic devices. In fact, there is no real method disclosed in Kurle et al., only FIG. 1A relied on by the Examiner, which shows raised portions between two layers of a wafer. The fact that a figure shows structure somewhat similar to what is discussed in Appellants' specification does not translate to a specified method, such as a method of packaging electronic devices that operate based on acoustic waves. Yet, the Examiner contends that one would look to the plasma display art, (Sasaki et al.) in order to find a reference that relates to a method step of a method for packaging electronic acoustic devices such as TFRs.

Even assuming arguendo that Kurle et al. teach all that is alleged, which Appellants submit it does not, the skilled artisan would not look to the plasma display panel art to solve the problems the have been addressed in, and solved by, the present application. In other words, one would not be motivated to combine Sasaki et al. with Kurle et al. Accordingly, as to be supported below, Appellants submit that the Examiner has (a) failed to make out a prima facie case of obviousness to combine Kurle et al. and Sasaki et al., essentially using Appellants' specification as a blueprint to piece together elements, and (b) has looked to a non-analogous art for a solution to the problem identified in the present application, and not in either Kurle et al. or Sasaki et al.

A. Rejection fails test for establishing prima facie case of obviousness.

Appellants direct the Examiner's attention to two recent cases decided by the Court of Appeals for the Federal Circuit (CAFC), In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed.Cir. 1999) and In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed.Cir. 2000). Both of these cases set forth very rigorous requirements for establishing a prima facie case of obviousness under 35 U.S.C. §103(a). To establish obviousness based on a combination of elements disclosed in the prior art, there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant. The motivation suggestion or teaching may come explicitly from one of the following:

(a) the statements in the prior art (patents themselves)
(b) the knowledge of one of ordinary skill art, or in some cases,
(c) the nature of the problem to be solved.

See Dembiczak 50 USPQ at 1614 (Fed.Cir. 1999). In Kotzab, the CAFC held that even though various elements of the claimed invention were present (in two separate embodiments of the same prior art reference), there was no motivation to combine the elements from the separate embodiments, based on the teachings in the prior art.

In order to establish a prima facie case of obviousness under 35 U.S.C. §103(a), the Examiner must provide particular findings as to why the two pieces of prior art are combinable. See Dembiczak 50 USPQ2d at 1617. Broad conclusory statements standing alone are not "evidence".

In order to provide motivation for combining Kurle et al. and Sasaki et al. to reject claim 1, on page 2 of the Office Action of April 3, 2003, the Examiner asserts:

> It would have been obvious . . . to lithographically form ridges in the method of Kurle because Sasaki teaches that it is a useful technique for forming ridges.

Appellants have read the entirety of Kurle et al. and Sasaki et al. several times and do not see how reading these references one of ordinary skill in art would think to combine Kurle et al. and Sasaki et al. FIG. 1A of Kurle et al. illustrates one step of a method for producing sensors, not packaging electronic devices. FIGS. 3 and 4 in Sasaki et al. describe various processes for building a plasma display panel for use in a digital video system, for example. The Examiner has not identified any teaching or suggestion, anywhere in Sasaki et al., in the process for manufacturing a gas discharge display panel, that would lead one skilled in the art to look to Sasaki et al. in order to figure out a way to package electronic acoustic devices such as TFRs, having acoustic (not light or optical) properties, for the purposes of reducing finer frit line width, limiting the effects of capacitive parasitic, each purpose of width influences acoustic properties, or to determine cavity depth independent of frit thickness, etc. Accordingly, Appellants respectfully submit that claim 1 is allowable for at least the additional reason that the Examiner has failed to establish a proper prima facie case of obviousness under 35 U.S.C. 103(a), in view of Dembiczak and Kotzab.

B. Examiner using Impermissible Hindsight.

The Examiner is using impermissible hindsight reconstruction to reject the claims. The Examiner has used the present application as a blueprint, selected a prior art method of wafer structure as the main structural device, and then searched other prior art for the missing elements without identifying or discussing **any specific evidence of motivation to combine,** other than providing conclusory statements regarding the knowledge in the art, motivation and obviousness. The Federal Circuit has noted that the PTO and the courts "cannot use hindsight reconstruction to **pick and choose among isolated disclosures in the prior art to deprecate the claimed invention,**" In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1780, 1783 (Fed. Cir. 1988),

and that the best defense against hindsight-based obviousness analysis is the rigorous application of the requirement for a showing of a teaching or motivation to combine the prior art references. Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight. Dembiczak, 50 USPQ2d at 1617. Appellants respectfully submit that claim 1 is allowable for at least this additional reason.

C. Examiner has not provided requisite motivation to combine references.

The Examiner has not provided the requisite evidence to support his allegation that there is motivation to combine Kurle et al. and Sasaki et al., so as to render obvious that which Appellants have described. The essential factual evidence on the issue of obviousness is set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966) and extensive ensuing precedent. The patent examination process centers on prior art and the analysis thereof. When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence **relevant** to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. See, e.g., McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the Graham factors).

The Examiner has not provided the requisite showing of a suggestion, teaching, or motivation to combine the prior art references to reject claim 1 in the present application. "The factual inquiry whether to combine references must be thorough and searching." Id. It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with. See, e.g., Brown & Williamson Tobacco Corp. v. Philip Morris Inc., 229 F.3d 1120, 1124-25, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000) ("a showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding'") (quoting C.R. Bard, Inc., v. M3 Systems, Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225,

1232 (Fed. Cir. 1998)); In re Dembiczak, 50 USPQ2d at 1617 ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998) (there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant); In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) ("'teachings of references can be combined only if there is some suggestion or incentive to do so.'") (emphasis in original) (quoting ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984)).

The Examiner must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

Accordingly, the Examiner has not adequately supported the selection and combination of Kurle et al. and Sasaki et al. to render obvious that which Appellants have described. The Examiner's conclusory statement "because Sasaki teaches that it is a useful technique for forming ridges" does not adequately address the issue of motivation to combine. This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). The Examiner must explain the reasoning behind his findings of motivation. Simply stating that the motivation for combining Kurle et al. and Sasaki et al. is "because Sasaki teaches that it is a useful technique for forming ridges" is an insufficient explanation for the alleged combination.

Further, the Examiner is reminded that deferential judicial review under the Administrative Procedure Act does not relieve the agency (in this case the USPTO) of its obligation to develop an evidentiary basis for its findings. To the contrary, the Administrative Procedure Act reinforces this obligation. See, e.g., Motor Vehicle Manufacturers Ass'n v. State Farm Mutual Automobile Ins. Co., 463 U.S. 29, 43 (1983) ("the agency must examine the relevant data and articulate a satisfactory explanation for its action including a 'rational connection between the facts found and the choice made.'") (quoting Burlington Truck Lines v. United States, 371 U.S. 156, 168 (1962). In this respect, since the examiner has not provided the requisite suggestion in the references to make his alleged combination, the Examiner rejects the precedent in In re Sung Lee, 23 USPQ2d 1780 (Fed. Cir. 2002).

In its decision on Lee's patent application, the Board rejected the need for "any specific hint or suggestion in a particular reference" to support the combination of the Nortrup and Thunderchopper references. Omission of a relevant factor required by precedent is both legal error and arbitrary agency action. See Motor Vehicle Manufacturers, 463 U.S. at 43 ("an agency rule would be arbitrary and capricious if the agency . . . entirely failed to consider an important aspect of the problem"); Mullins v. Department of Energy, 50 F.3d 990, 992 (Fed. Cir. 1995) ("It is well established that agencies have a duty to provide reviewing courts with a sufficient explanation for their decisions so that those decisions may be judged against the relevant statutory standards, and that failure to provide such an explanation is grounds for striking down the action."). As discussed in National Labor Relations Bd. v. Ashkenazy Property Mgt. Corp., 817 F.2d 74, 75 (9th Cir. 1987), an agency is "not free to refuse to follow circuit precedent." Appellants submit that the Examiner has failed to provide a specific hint or suggestion in any of Kurle et al. and Sasaki et al. to support the alleged combination. In light of the weight of the above precedent, and in addition to the reasons in A. and B above, Appellants respectfully submit that claim 1 is allowable.

D. Sasaki et al. is Non-analogous art.

Electronic devices fabricated in a large scale integrated (LSI) manner by thin film deposition, etching, etc., need to be packaged so as to be easily handled, and so as to be reliable in the variety of environmental conditions that are typically present in electronic systems. For devices based on acoustic waves or mechanical motion, the part of the device that contains these acoustic waves must be isolated from intimate contact with packaging material, or the acoustic wave may be corrupted. The isolation can be achieved by forming a desired sized cavity of desired depth over the devices. It is preferred to form these cavities at the wafer scale, lowering the cost per part. One way to do this is to prepare a capping wafer to be bonded to a wafer that is prepared with devices. These wafers can then be bonded together, and thereafter the devices can be singulated (e.g., separated into individual devices).

The present invention thus provides a way to package electronic, acoustic devices such as TFRs by forming raised areas between substrate and a cap wafer that results in a finer frit line width, as compared to wafers manufactured in Kurle et al., for example. Kurle et al. is directed to a method of producing wafers of a wafer stack. The field of endeavor is thus methods of packaging or producing devices with thin bonding regions.

Sasaki et al. is directed to a gas discharge panel and method for manufacturing the same, for use in a plasma display such as a plasma display TV. Sasaki et al.'s process is of special interest in developing plasma display panels (PDPs) with improved brightness, and quality of display (e.g., less deterioration due to a gap perforating division walls between compartments 112, which are light emitting regions, see paragraphs [0027] and [0176] of Sasaki et al). Sasaki et al. has nothing to do with Appellants' field of endeavor.

> The determination that a reference is from a non-analogous art is ... twofold. First, we decide if the reference is within the field of the inventor's endeavor. If it is not, we proceed to determine whether the reference is reasonably pertinent to the particular problem with which the inventor was involved. In re Wood, 202 USPQ 171, 174 (C.C.P.A. 1979).

Sasaki et al. is also not reasonably pertinent to Appellants' invention, or to Kurle et al., for that matter.

> A reference is reasonably pertinent if ... it is one which, because of the matter with which it deals, logically would have commended itself to the inventor's attention in considering his problem.... If a referenced disclosure has the same purpose as the claimed invention, the reference relates to the same problem ... if it is directed to a different purpose, the inventor would accordingly have had less motivation or occasion to consider it. In re Clay, 23 USPQ.2d 1058, 1060-61 (Fed. Cir. 1992).

Sasaki et al., at best, discloses a method of manufacturing a gas discharge panel. The present application provides a method for packaging acoustic electronic devices. FIG. 1A in Kurle et al' is directed to manufacturing a sensor of a wafer stack. The inventors of the present invention would not look to Sasaki et al. to solve the problems identified by the present invention (Kurle et al. certainly does not address the problem), since Sasaki et al. provides no indication of the same purpose as the claimed invention---packaging electronic, acoustic devices as recited in claim 1. Appellants respectfully submit that claim 1[1] is allowable for this additional reason.

II. Issue 2: Are claims 8, 9 and 12 rendered obvious by Kurle et al. in view of Sasaki et al.?

The Examiner already admits that Kurle et al does not teaching anything related to the trenching of recesses and printing of material into the recesses. In fact, the rejection is not clear as to what exactly Kurle et al. teaches with respect to claim 8 (see page 3 of final Office Action, April 3, 2003). Appellants' submit that Sasaki et al. does not disclose or suggest "trenching recesses into the cap wafer surface at areas near the perimeter of a desired cavity region" and "printing material into the recesses and planarizing it such that each filled recess is flush with the cap wafer surface" and "etching away the cap wafer surface, except for the areas of the original recesses, so

[1] Claim 5 is also allowable for any of the above reasons by virtue of its dependency from claim 1, but is held by Appellants as being separately patentable for the reasons set forth below in III.

that the material forms the raises ridges that are bonded to the substrate surface, as recited in independent claim 8

Referring to Sasaki et al., Figs. 3(a)-3(e), Sasaki et al. shows a process in which division walls may be formed and frit glass then applied to the top of the division walls. However, Sasaki et al. does not disclose trenching recesses into the cap wafer surface. Referring to Figs. 3(c), a resist 64 is applied over a dielectric film 63. Then, light is used to pattern the dielectric film. Fig. 3(d) shows the formation of the division walls 65. Finally, the raised division walls become evident upon the removal of the resist 64.

However, Figs. 3(a)-3(e) do not describe a process in which (a) recesses are trenched in the cap wafer surface, (b) material is printed into the recesses and planarized, and then (c), the cap wafer surface is etched. For at least these reasons, the rejection should be withdrawn and claim 8 indicated as allowable, as the combination of Kurle et al. and Sasaki et al. fail to teach each feature recited in claim 8. Claims 9 and 12, dependent upon independent claim 8, are likewise allowable over the cited references at least for the reasons given above with respect to independent claim 8.

Notwithstanding the above, the rejection of claim 8 is also deficient as against the weight of case precedent directed to obviousness rejections under 35 U.S.C. §103. In order to provide motivation for combining Kurle et al. and Sasaki et al. to reject claim 8, on page 4 of the Office Action of April 3, 2003, the Examiner asserts:

> It would have been obvious to use the method of Sasaki to form the raised ridges in the method of Kurle because Sasaki teaches that it is a useful technique for forming ridges to bond two substrates together with glass frit.

Appellants submit that, in addition to the technical distinctions above, the Kurle et al./Sasaki et al. combination fails to set forth a proper prima facie case of obviousness. Appellants have read the entirety of Kurle et al. and Sasaki et al. several times and do not see how reading these references one of ordinary skill in art would think to combine Kurle et al. and Sasaki et al. Accordingly, Appellants respectfully submit that claim 8 is allowable for at least the additional reason that the Examiner has failed to establish a

proper prima facie case of obviousness under 35 U.S.C. 103(a), in view of Dembiczak and Kotzab, as discussed in I. (A) above.

Additionally, and as elucidated in detail in I. (B), the Examiner has used impermissible hindsight by combining Kurle et al. and Sasaki et al. without evidence of such a suggestion, teaching, or motivation, using the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight. Further, the Examiner has attempted to apply a non-analogous reference which is neither within the field of the inventor's endeavor, nor reasonably pertinent to the particular problem with which the inventor was involved (see I. (D) above). Claim 8 is thus allowable for these additional reasons. Claims 9 and 12[2], dependent upon independent claim 8, are likewise allowable over the cited references at least for the reasons given above with respect to independent claim 8.

III. Issue 3: Are claims 5 and 10 rendered obvious by Kurle et al. in view of Sasaki et al.?

Claims 5 and 10 are separately patentable because neither Kurle et al. nor Sasaki et al. teach or suggest a linewidth of the frit being less than 125 μm. The Examiner indicates that Kurle discloses a linewidth of 500 microns (col. 3, line 26), which is greater than125 microns. Yet the Examiner alleges that Sasaki et al. teaches that a linewidth may be 40 microns (page 12, Paragraph [0285].

However, Sasaki et al. refers to a linewidth of 40 in describing FIG. 13, which "shows a case where maximum particle size D of the material such as the filler included in the bonding members 15 does not exceed the width W of the division walls 7." (Page 12, Paragraph [0283]). The bonding material, or filler, which is contained within the frit

[2] Claims 10 and 11 are also allowable for any of the above reasons in II. by virtue of their dependency from claim 8, but are held by Appellants as being separately patentable for the reasons set forth below in III and IV.

glass and is not the frit, cannot be construed as a frit linewidth less than 125 microns, as recited in claims 5 and 10. The filler is not a frit.

Even if Sasaki arguably taught such a feature, which Appellants submit it does not, there is no motivation to combine Sasaki et al. with Kurle et al. The frit strips shown in the Kurle et al. are typically applied with a screen printed process, and a resulting minimal linewidth is typically quite large, greater than 125 microns, as indicated in Kurle et al. This is undesirable, since these substrate surfaces (to which the cap wafer is to be attached to) contain many electrical components or sensors such as thin film resonator (TFR) components and/or filter components.

From these components or devices, interconnects must be run under the frit seal in the cap wafer, and in the above example in Kurle et al., an additional 500 extra microns of "runner" are needed in order to get underneath the frit. This introduces resistive losses and additional inductive and capacitive parasitics that limit device performance. Additionally, the excessive frit width of the prior art also introduces a significant increase in die size; thus there are fewer sensory devices produced per wafer.

As seen in Fig. 3(b) of the present invention, by providing a cap wafer surface 302 that has been etched so as to form raised ridges 304 onto which the sealing 310 is applied, the frit linewidth dimension is reduced to a value less than X. Therefore the sealing material 310 that is printed on the raised ridge 304 is subject to a surface tension to "hold" the sealing material 310 into higher, thinner line dimensions.

Additionally, any excess material will flow off of the ridge 304. This is advantageous with respect to minimizing the frit linewidth (< X) and reducing capacitive parasitics, since not much of the surface area of the cap wafer surface 302 is in contact with the substrate surface and electrical components (not sown) attached thereto. Thus, shorter electrical runners (not shown in Figs. 3(a) and 3(b) are needed, and therefore less of the runner is subjected to undesirable parasitics. In addition to a frit linewidth less than 125 microns being absent in Kurle et al or Sasaki et al., the advantages of having a frit linewidth less than 125 microns are not even tangentially addressed in

either of Kurle et al. or Sasaki et al. Claims 5 and 10 are thus separately patentable for the reasons set forth above.

IV. Issue 4: Is claim 11 rendered obvious by Kurle et al. in view of Sasaki et al.?

Claim 11 recites that "after the recesses are formed and the recesses are filled, the raised ridges are fabricated by etching the surrounding cap wafer surface surrounding each filled recess". Appellants submit that claim 11 is separately patentable in that this feature is not taught by either Kurle et al. nor Sasaki et al.

Kurle et al is completely silent on forming recesses of any kind. Appellants submit. Referring to Fig. 3(c), of Sasaki et al., a resist 64 is applied over a dielectric film 63. Then, light is used to pattern the dielectric film. Fig. 3(d) shows the formation of the division walls 65. Finally, the raised division walls become evident upon the removal of the resist 64. This process does not teach or suggest (a) forming recesses of any kind, (b) filling the recess, and (c) fabricating the raised ridges by etching the filled recess. Accordingly, claim 11 is thus separately patentable for this reason.

CONCLUSION

For all the reasons set forth above, the present invention as recited in Appellants' pending claims 1, 5 and 7-12 are not anticipated, nor rendered obvious to one skilled in the art as asserted by the Examiner. Accordingly, it is respectfully submitted that the claimed invention should properly be patentable over the cited art. It is therefore respectfully requested that this Appeal be granted by the panel and that the Examiner be reversed.

In the event that any matters remain at issue in the application, the Examiner is invited to contact Matthew J. Lattig at (703) 668-8026 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____ 45 274
Gary D. Yacura, Reg. No. 35,416

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

GDY/MJL

Attached: (9) Appendix: Pending claims of record

(9) APPENDIX:

1. A method of packaging electronic devices that operate based on acoustic waves, comprising the steps of:

providing a cap wafer having a surface;

lithographically forming raised ridges on the cap wafer surface at areas near a perimeter of a desired cavity region so that the raised ridges are a contiguous part of said cap wafer;

printing a glass frit material on the raised ridges; and

bonding, via said glass frit material at each raised ridge, the cap wafer surface to a substrate surface containing electronic devices,

each raised ridge using surface tension to hold the glass frit to a higher and thinner frit line width dimension, and to prevent lateral flow of the glass frit, than if the frit were deposited directly on a flat cap wafer surface without lithographically formed raised ridges .

5. (Currently Amended) The method of claim-41, wherein a linewidth of the frit is less than 125 μm.

7. The method of claim 1, wherein bonding areas when the raised ridges are bonded form a continuous perimeter around the device, so that a hermetic seal is formed.

8. A method of packaging electronic devices operating based on acoustic waves, comprising the steps of:

providing a cap wafer having a surface;

trenching recesses into the cap wafer surface at areas near the perimeter of a desired cavity region;

printing material into the recesses and planarizing it such that each filled recess is flush with the cap wafer surface; and

etching away the cap wafer surface, except for the areas of the original recesses, so that the material forms the raised ridges that are bonded to the substrate surface.

9. The method of claim 8, wherein each raised ridge is formed slightly inboard from the perimeter of a desired cavity region, each raised ridge composed of a glass frit material for bonding the cap wafer to the substrate.

10. The method of claim 9, wherein a linewidth of the frit is less than 125 μm.

11. The method of claim 8, wherein, after the recesses are formed and the recesses are filled, the raised ridges are fabricated by etching the surrounding cap wafer surface surrounding each filled recess.

12. The method of claim 8 wherein the ridges form a continuous perimeter around a cavity region such that a hermetic seal is made when the cap wafer is bonded to a wafer of an electronic device.